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The listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1. (Previously Presented) A configurable real time video processor arranged to provide a single synchronized display video stream having a single display video format to a display unit having an associated set of display attributes from a number of video streams of different video formats, comprising:

a number of ports each of which is configured to receive one of the video streams at a corresponding input video stream clock rate;

a number of adaptive image converter units each coupled to an associated one of the ports for converting the corresponding input video data stream to a corresponding converted video stream having the single display video format that is based upon the set of display attributes; and

a frame rate conversion unit configured to synchronize each converted data stream to a selected output frame rate .

2. (Previously Presented) A configurable real time video processor as recited in claim 1, further comprising:

a format converter unit coupled to one of the ports arranged to convert a corresponding video stream to a progressive video stream, if needed.

3. (Previously Presented) A configurable real time video processor as recited in claim 1, further comprising:

an image compositor unit arranged to combine any number of the converted video streams to form a composited video stream;

an image enhancer unit arranged to enhance the composited video stream to form an enhanced video stream;

a display unit interface arranged process the enhanced video stream to form the display data; and

a memory unit bi-directionally coupled to each of the image converter units and the image compositor arranged to store selected portions of selected ones of the video streams from the image converter units and to provide the selected portions to the image compositor unit as needed.

4. (Currently Amended) A configurable real time video processor as recited in claim 1, wherein the output frame rate is ~~can be~~ selectively locked to any of the input video data stream clock rates or a ratio of the input video data stream clock rates.

5. (Cancelled)

6. (Cancelled)

7. (Previously Presented) A configurable real time video processor as recited in claim 4, wherein the selected frame rate is a free running frame rate.

8. (Previously Presented) A configurable real time video processor as recited in claim 1, wherein the ports include,

a video receiver port arranged to receive video data at a video clock rate;

a bi-directional network interface arranged to receive network data from network applications on a network and transmit data to the network from the real time video processor at a network data clock rate;

and

a user interface port arranged to receive user input commands at a user interface clock rate.

9. (Previously Presented) A configurable real time video processor as recited in claim 1, wherein the video processor is an integrated circuit.

10. (Previously Presented) A configurable video processor as recited in claim 1, wherein the display attributes are Extended Display Identification Data (EDID).

11. (Currently Amended) A configurable real time video processor as recited in **claim 3** ~~claim 6~~, wherein the display **unit** interface further comprises:

an interlacer unit arranged to interlace a progressive scan image when the display unit is an interlaced type display unit; and

a progressive scan bypass unit arranged to bypass the interlacer when the display unit is a progressive scan type display unit.

12. (Previously Presented) A method of adaptively providing a single synchronized display video stream having a single display video format to a display unit having an associated set of display attributes from a number of video streams of different video formats by a video processor, comprising:

receiving the input video data streams at a corresponding one of a number of input ports at an associated input video stream clock rate

converting the corresponding video stream to a converted video stream having the single display video format; and

synchronizing each converted data stream to an output frame rate.

13. (Previously Presented) A method as recited in claim 12, further comprising:

converting a corresponding video stream to a progressive video stream, if needed.

14. (Previously Presented) A method as recited in claim 12, further comprising:

combining any number of the converted video streams to form a composited video stream;

enhancing the composited video stream to form an enhanced video stream;

processing the enhanced video stream to form the display data; and

storing selected portions of selected ones of the video streams from the image converter units and to provide the selected portions to the image compositor unit as needed

15. (Currently Amended) A method as recited in claim 13, further comprising:

wherein the output frame rate ~~can be~~ is synchronized to any of the input video data stream clock rates or a ratio of the input video data stream clock rates

16. (Cancelled)

17. (Cancelled)

18. (Previously Amended) A method as recited in claim 15, wherein the selected output frame rate is a free running frame rate.

19. (Previously Presented) A method as recited in claim 12, wherein the ports include,

a video receiver port arranged to receive video data at a video clock rate;

a bi-directional network interface arranged to receive network data from network applications on a network and transmit data to the network from the real time video processor at a network data clock rate;

and

a user interface port arranged to receive user input commands at a user interface clock rate.

20. (Previously Presented) A method as recited in claim 12, wherein the video processor is an integrated circuit.

21. (Original) A method as recited in claim 12, wherein the display attributes are Extended Display Identification Data (EDID).

22. (Original) A method as recited in claim 21, further comprising:

interlacing a progressive scan video image when the display unit is an interlaced type display unit; and

bypassing the interlacing when the display unit is a progressive scan type display unit.

23. (Previously Presented) Computer program product for adaptively providing a single synchronized display video stream having a single display video format to a display unit having an associated set of display attributes from a number of video streams of different video formats by a video processor, comprising:

computer code for receiving one of the video streams at one of a number of input ports at an associated input video stream clock rate

computer code for converting the corresponding video stream to a converted video stream having the single display video format;

computer code for synchronizing each converted data stream to an output frame rate; and

computer readable medium for storing the computer code.

24. (Currently Amended) Computer program product as recited in claim 23, wherein the output frame rate ~~can be~~ is selectively synchronized to any of the input video data stream clock rates or a ratio of the input video data stream clock rates.

25. (Previously Presented) Computer program product as recited in claim 23, further comprising:

computer code for combining any number of the converted video streams to form a composited video stream;

computer code for enhancing the composited video stream to form an enhanced video stream;

computer code for processing the enhanced video stream to form the display data; and

computer code for storing selected portions of selected ones of the video streams from the image converter units and to provide the selected portions to the image compositor unit as needed

26. (Cancelled)

27. (Cancelled)

28. (Cancelled)

29. (Previously Presented) Computer program product as recited in claim 24, wherein the selected output frame rate is a free running frame rate.

30. (Previously Presented) Computer program product as recited in claim 23, wherein the ports include,

a video receiver port arranged to receive video data at a video data clock rate;

a user interface port arranged to receive user input commands at a user interface clock rate, and

a bi-directional network interface arranged to receive network data from network applications on a network and transmit data to the network from the real time video processor at a network data clock rate.

31. (Original) Computer program product as recited in claim 23, wherein the data processor is an integrated circuit.

32. (Original) Computer program product as recited in claim 23, wherein the display attributes are Extended Display Identification Data (EDID).

33. (Original) Computer program product as recited in claim 30, further comprising:

computer code for interlacing a progressive scan video image when the display unit is an interlaced type display unit; and

computer code for bypassing the interlacing when the display unit is a progressive scan type display unit.